AMENDMENTS TO THE CLAIMS

Please add or amend the claims to read as follows, and cancel without prejudice or disclaimer to resubmission in a divisional or continuation application claims indicated as cancelled:

1. (currently amended) A method [comprising] comprising:

synchronizing interrupts to a processor with signals from a slot timer of a wireless link synchronization unit connected to said [processor] processor, wherein during the execution by the processor of a scheduled time-dependent function, processor interrupts are prohibited.

2. (cancelled)

3. (previously presented) The method as in claim 1, comprising scheduling interrupts to said processor in advance of slot signals issued by said wireless link synchronization unit

4. (original) The method as in claim 1, comprising dividing a function into at least two or more segments wherein a segment may be processed to completion by said processor within the time available in a slot.

5. (original) The method as in claim 4, comprising dividing a background function into two or more segments.

6. (withdrawn) A method comprising prohibiting interrupts of a processor during a slot other than interrupts by a command scheduled for processing during said slot.

7. (withdrawn) The method as in claim 6, comprising scheduling, prior to the start of said slot, said command to be processed by said processor during said slot.

8. (withdrawn) The method as in claim 7, wherein said scheduling comprises selecting a background command to be processed by said processor during said slot.

9. (withdrawn) The method as in claim 8, wherein scheduling said background command comprises selecting a load estimation command.

10. (withdrawn) The method as in claim 8, wherein said selecting said background command comprises selecting a segment of said background command to be processed during said slot.

11. (withdrawn) The method as in claim 6, comprising selecting said command to be processed by said processor on the basis of a pre-determined priority among commands waiting to be processed by said processor.

12. (withdrawn) The method as in claim 6, comprising masking a signal of a slot timer during a processing of a transmit command.

13. (withdrawn) The method as in claim 6, comprising storing in a data storage unit an indication of commands waiting to be processed by said processor.

14. (withdrawn) The method as in claim 13, comprising storing in a second data storage unit an indication of a slot timer signal that may interrupt said processor during said slot.

15. (withdrawn) The method as in claim 14, comprising comparing a value stored in a designated position of said data storage unit with a value stored in a designated position of said second data storage unit.

16. (cancelled)

17. (cancelled)

18. (cancelled)

19. (withdrawn) A method comprising delaying during a slot an interruption of a processor.

20. (withdrawn) The method as in claim 19, comprising scheduling, prior to the start of said slot, a command to be processed by said processor during said slot.

21. (withdrawn) The method as in claim 19, wherein said delaying comprises delaying an interrupt of said processor during the processing of a background command.

22. (withdrawn) The method as in claim 19, comprising dividing a background command into segments, said segments capable of being processed to completion within the time available in a slot.

23. (currently amended) An article [comprising] comprising:

a data storage unit having stored thereon instructions that when executed by a processor, result in synchronizing interrupts to a processor with signals from a slot timer of a wireless link synchronization unit connected to said [processor.] processor, wherein during the execution by the processor of a scheduled time-dependent function, processor interrupts are prohibited.

24. (cancelled)

25. (previously presented) The article as in claim 23, wherein said instructions further result in scheduling interrupts to said processor in advance of slot signals issued by said wireless link synchronization unit.

26. (currently amended) A communication device comprising:

a dipole antenna; and a

a state machine to synchronize interrupts to a processor with timing signals from a slot timer of a wireless link synchronization unit connected to said [processor.]

processor, wherein during the execution by the processor of a scheduled time-dependent function, processor interrupts are prohibited.

27. (cancelled)

28. (original) The communication device as in claim 26, comprising a register to store an indication of a background function waiting to be processed.

29. (withdrawn) An apparatus comprising:

a host; and

a controller,

said controller to prohibit interrupts of a processor during a slot other than by a command scheduled for processing during said slot.

30. (withdrawn) The apparatus as in claim 29, wherein said controller is to schedule, prior to the start of said slot, said command to be processed by said processor during said slot.

31. (withdrawn) The apparatus as in claim 29, wherein said controller is to select a background command to be processed by said processor during said slot.

32. (cancelled)

33. (cancelled)

34. (cancelled)

35. (withdrawn) A device comprising a controller to delay an interrupt of a processor during a slot.

36. (withdrawn) The device as in claim 35, said controller to schedule, prior to the start of said slot, a command to be processed by said processor during said slot.

37. (withdrawn) The device as in claim 35, said controller to divide a background command into segments, said segments capable of being processed to completion by said processor within the time available in said slot.